IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Jeffrey Craig et al.	Confirmation No.:	1181
Patent No.:	7,246,268 B2	Issue Date:	July 17, 2007
Application No.:	10/051,833	Group Art Unit:	2114
Filing Date:	January 16, 2002	Examiner:	Contino, Paul F.
For:	Method and Apparatus for Dynamic Degradation Detection	Attorney Docket No.:	250543-41100

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

Column 12:

Line 34 (claim 15, line 2), after "device,", delete "and", insert -- an --.

Support for the above change to claim 15 appears in application claim 33.

The requested corrections are for errors that appear to have been made by the Office. Therefore, no fee is believed to be due for this request. Should any fees be required, however,

please charge such fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

9/25/07
Date

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What is claimed is:

1. A memory system for storing information, the memory system comprising:

a first plurality of spare units of erase on a first chip;

a second plurality of spare units of erase on a second chip;

a first storage element on the first chip, the first storage element containing a first counter and a first threshold, the first counter indicating a number of spare units of erase on the first chip which have not yet been reassigned;

a second storage element on the second chip; the second storage element containing a second counter and a second threshold, the second counter indicating a number of spare units of erase on the second chip which have not yet been reassigned;

a controller, the controller updating the first counter each time a spare unit of erase of the first plurality of spare units of erase is reassigned, the controller comparing the first counter to the first threshold value, the controller updating the second counter each time a spare unit of erase of the second plurality of spare units of erase is reassigned, the controller comparing the second counter to the second threshold value, the controller generating an end-of-life indicator when either the first counter reaches the first threshold or the second counter reaches the second threshold; and

wherein the memory system operates in conjunction with a host system and the controller reassigns a spare unit of erase in response to a request from the host system.

2. The memory system of claim 1 wherein when the controller compares the first counter to the first threshold value to determine if the memory system is in an end-of-life the condition, the controller determines that the memory system is in the end-of-life condition when a value of the first counter is less than or equal to the first threshold value.

3. The memory system of claim 1 wherein the controller attempts to write data to a first unit of erase on the first chip, and determines if the first unit of erase is worn.

4. The memory system of claim 3 wherein when it is determined that the first unit of erase is worn, the controller reassigns a first spare unit of erase included in the first plurality of spare units of erase as the first unit of erase.

5. The memory system of claim 4 wherein the controller writes the data into the reassigned first spare unit of erase.

6. The memory system of claim 1 wherein the controller attempts to write data to a first unit of erase on the first chip to determine if the first unit of erase is defective.

7. The memory system of claim 6 wherein when it is determined that the first unit of erase is defective, the controller reassigns a first spare unit of erase included in the first plurality of spare units of erase as the first unit of erase.

8. The memory system of claim 7 wherein the controller writes the data into the reassigned first spare unit of erase.

9. The memory system of claim 1 wherein an individual one of the first plurality of spare units of erase is a sector, and an individual one of the second plurality of spare units of erase is a spare sector.

10. The memory system of claim 1 further including:

a non-volatile memory, wherein the first plurality of spare units of erase, the second plurality of spare units of erase, and the first storage element are included in the non-volatile memory.

11. The memory system of claim 1 wherein the memory system is a non-volatile memory system.

12. The memory system of claim 1 wherein the memory system is one of a PC card, a CompactFlash card, a Multi-Media card, a MemoryStick card, and a Secure Digital card.

13. The system of claim 1 wherein the host system is arranged to capture information and to attempt to store the information in the memory system.

14. The system of claim 13 wherein the information is one of audio information and wireless information.

15. The system of claim 14 wherein the host system is one of a cellular communications device, an audio player, and a video player.

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,246,268 B2

APPLICATION NO. : 10/051,833

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INVENTOR(S) : Jeffrey Craig and John S. Mangan

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12:
Line 34 (claim 15, line 2), after "device,", delete "and", insert -- an --.

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